

**ABSTRACT OF THE DISCLOSURE**

In a method and apparatus for controlling a dual-slope integrator circuit, a reset signal is provided to a reset input of the integrator circuit to maintain a reset state of an integrating capacitor for a predetermined reset time period in response to an original input signal. A delayed input signal is simultaneously generated by introducing a predetermined delay period into the original input signal, the delay period being longer than the reset time period. With reference to the original input signal and the delayed input signal, a trigger signal is provided to an integrator input of the integrator circuit for enabling charging operation of the integrating capacitor during a charging period that starts from the end of the reset time period and that terminates at a lagging edge of the delayed input signal.